REMARKS

The office action indicates that Rajski can still be applied for "at least claim 16." Thus, it is understood that the rejection based on Rajski is withdrawn as to all other claims.

As to claim 16, it should be noted that claim 16 calls for gates arranged to handle "any number of scan chains with unknown logic values." Clearly, Rajski teaches no such system. In the material relied on by the Examiner under the heading 2. FS Compactor, it is explained that no odd number of errors or two errors injected at the same time or in different time frames can mask each other completely. Also, single errors injected in each scan propagate to outputs in a different recognizable pattern. Thus, it is clear that Rajski's system cannot handle any number of scan chains with unknown values.
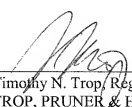
This is made even more clear on page 3 under the heading 3. Error Masking in the Absence of X States. There, it is explicitly stated that, as shown above, detection of errors in multiplicity 4 and higher even multiplicity is not guaranteed. In the ensuing section, Error Masking in the Presence of X States, it is explained that, because of the basic properties of polynomials, a single X state injected into the compactor, either at the same scan out cycle or another one, will not be able to mask entirely the error syndrome. Clearly, Rajski concedes that his compactor does not meet the claimed limitation.

Therefore, reconsideration is requested.

With respect to the rejection under Section 102, based on the published application of Mitra and Kim, it is noted that the inventors of that application and the inventors of this application are the same. Therefore, a Section 102(e) cannot apply since it requires an application for patent "by another filed." The cited Mitra application is not by another filed, but, instead, both applications are by the exact same inventors. Therefore, reconsideration would be appropriate.

Respectfully submitted,

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